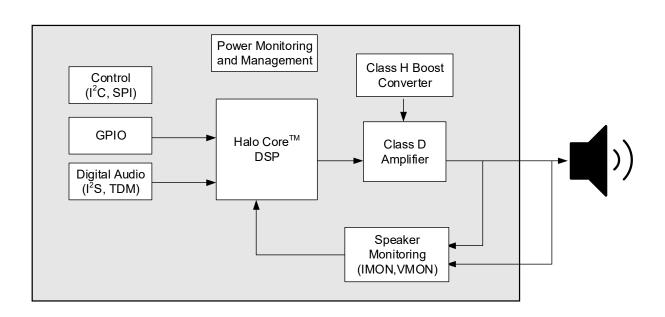


11 V Boosted Mono Class D Amplifier with DSP

Speaker Amplifier Features	System Protection Features
Class D architecture with adaptive output stage reduces	IC thermal self-protection against overtemperature
idle power consumption and switching losses	 System supply rail reactive brownout system protection
Digital input supports I ² S or TDM serial audio	 Speaker current sensing via integrated
 5.3 W @ 1% THD+N into 8 Ω (1 kHz, VP = 4.3 V) 	current-monitoring sense resistor
 6.0 W @ 10% THD+N into 8 Ω (1 kHz, VP = 4.3 V) 	 Current and voltage monitor data on I²S/TDM interface
 Shared boost rail supply option 	DC input watchdog
 11 V amplifier supply maximum voltage 	
 Programmable digital volume and amplifier gain 	Digital Boost Converter Features
 Low idle channel noise: 9 µVrms (A-weighted) 	 Class H envelope-tracking boost supply
 –78 dB THD+N @ 1 W into 8 Ω (1 kHz, VP = 3.6 V) 	 Integrated boost and rectification FETs
 Advanced ΔΣ closed-loop architecture 	 High-bandwidth digital control loop
 Amplifier short-circuit protection 	2 MHz switching frequency
Multidevice synchronization	 Synchronous rectification in Boost Active Mode
	Pulse-skipping mode for improved efficiency during low
Configuration and Diagnostic Features	power quiescent operation
Diagnostic signal generator for rapid test development	 Programmable boost voltages of up to 11 V
 Soft reset via I²C/SPI control port 	
Hardware reset via pin	
·	







General Description

The CS35L42 integrates a high-performance mono audio amplifier, 130 MCPS Halo CoreTM DSP, and amplifier voltage boost converter to enable an easy-to-integrate speaker playback solution performing both robust transducer protection and enhancement functions.

The integrated DSP performs all required audio path equalization, enhancement, and protection while off-loading the application processor, allowing an overall lower system power state during audio playback. PLL-based internal clock generation from the audio serial timing supports a range of sample rate options from 44.1–96 kHz without an additional external MCLK reference clock source, further easing system integration.

The Class D amplifier features an advanced closed-loop architecture providing superior power supply rejection ratio (PSRR), and a complementary output stage. The elevated VBST supply generated by the boost converter allows the CS35L42 to deliver up to 5.3 W into an 8 Ω speaker and 5.5 W into a 6 Ω speaker at 1% THD+N.

The digitally controlled boost converter boosts standard-voltage lithium-ion and lithium-polymer battery voltages up to 11 V. The boost converter's output voltage automatically tracks the audio using an integrated Class H algorithm or can be configured via software control interface. A configurable weak-drive mode allows automatic reduction of power consumption during idle (low-output power) conditions by reducing switching losses.

The enhancement algorithms are designed to provide flexible tuning capability for a high performance portable audio system. Speaker protection algorithms are complete and robust, requiring minimal parameter settings to configure for the specific speaker and the associated speaker back volume and acoustics. Cirrus Logic provides an optimized tool chain to facilitate creating and programming the appropriate coefficients for enhancement and speaker protection for development and mass production. Cirrus Logic also provides Android device drivers for the CS35L42.

The CS35L42 includes self-protection and system-protection features as well. The boost and amplifier stage are protected against short circuits. IC overtemperature shutdown protection is provided in hardware.

The supply voltage is continuously monitored. The boost converter and amplifier gain are automatically adjusted to preserve the supply voltage according to programmable voltage/current load-shedding setpoints. The supply voltage protection adjustment of the amplifier is integrated with the IC and speaker thermal protection, ensuring seamless coordination of gain rollback.

Multidevice synchronization enables parameters such as gain levels to be cross-communicated with other Cirrus Logic audio and haptics amplifiers in the same system, maintaining stereo image balance and total system current budget.

The CS35L42 is available in a commercial-grade 0.4-mm pitch, 30-ball wafer level chip scale package for operation from -40° to +85°C. See Section 12 for ordering information.



1 Pin Descriptions

These sections show pin assignments and describe pin functions.

1.1 WLCSP Package Drawing (Top View, Through Package)

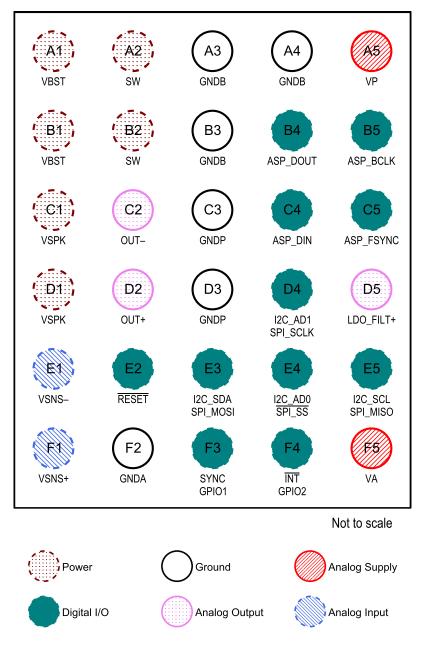


Figure 1-1. WLCSP 30-Ball Package Assignments (Top View, Through-Package)



1.2 Pin Descriptions

Table 1-1. WLCSP Pin Descriptions

Pin Name	Ball #	Power Supply	I/O	Description	Internal Connection	State at Reset
ASP_BCLK	BCLK B5 VA I/O Audio Serial Port Bit Clock. Serial shift clock for the interface.		Weak pull-down	Weak pull-down		
ASP_DIN	C4	VA	I/O	Audio Serial Port Data Input. I2S and TDM serial audio input.	Weak pull-down	Weak pull-down
ASP_DOUT	B4	VA	0	Audio Serial Port Data Output. I ² S and TDM serial audio data output.	Weak pull-down	Weak pull-down
ASP_FSYNC	C5	VA	I/O	Audio Serial Port Frame Sync Clock. Identifies the start of each serialized PCM data word and indicates which channel, left or right, is active on the serial PCM audio data lines or indicates the start of each TDM frame.	Weak pull-down	Weak pull-down
GNDA	F2	_	_	Analog and Digital Ground. Ground reference for the analog and digital portions of the IC.	_	_
GNDB	A3, A4, B3	—	_	Boost Converter Ground. Ground reference for the internal boost converter.	_	—
GNDP	C3, D3			Power Ground. Ground reference for the boost converter and Class D amplifier's output stage.	—	_
I2C_AD0/SPI_SS	E4	VA	I	I ² C Slave Device Address Select 0. Used with I2C_AD1, connected to VA or GNDA, to select between four possible addresses. SPI Control-Port Slave Select. Active-low SPI Slave Select	_	_
I2C_AD1/ SP[SCLK	D4	VA	I	input. I ² C Slave Device Address Select 1. Used with I2C_AD0, connected to VA or GNDA, to select between four possible addresses.	_	_
				SPI Control-Port Clock. SPI clock input.		
I2C_SCL/ SPI_MISO	E5	VA	I/O	I ² C Control-Port Clock. Clock input for the I ² C interface. SPI Control-Port Master In Slave Out. SPI data output.	—	Hi-Z
I2C_SDA/ SPI_MOSI	E3	VA	I/O	I ² C Control-Port Data. Data input/output for the I ² C interface. SPI Control-Port Master Out Slave In. SPI data input.	—	Hi-Z
INT/GPIO2	F4	VA	I/O	Interrupt. Configurable as an open-drain or CMOS (push-pull), programmable interrupt output. General Purpose Input/Output Pin. Programmable GPIO with alternate functions for MCLK input.	_	Hi-Z
LDO_FILT+	D5	VA	0	Digital Core LDO Output. Decoupling point for the integrated LDO providing power to the digital core circuitry on the CS35L42.		_
OUT+	D2	VSPK	0	Differential Audio Output. Internal Class D amplifier output.		_
OUT-	C2	VSPK	0	Differential Audio Output. Internal Class D amplifier output.	_	
RESET	E2	VA	I	Reset. If this pin is driven low, the device enters a low power mode, all outputs are set to Hi-Z, all register values are set to their default settings and all DSP volatile memories (RAM) are invalidated.	_	_
SW	A2, B2	VBST	l	Boost Switch. Input to internal boost FETs. Connect to L_{BST} inductor.	_	
SYNC/GPI01	F3	VA	I/O	Multidevice Synchronization Data. Serial data bus for communicating operational state information across devices in multi-channel applications. General Purpose Input/Output Pin. Programmable GPIO with alternate functions for MCLK input.	_	Hi-Z
VA	F5		I	Analog Power. Power supply for internal analog and digital sections.		_
VBST	A1, B1	_	0	Boosted Supply from Boost Converter. Internal boost converter output.	_	_



Pin Name Ball # Power I/O Description		Description	Internal Connection	State at Reset		
VP	A5	_	I	Boost Converter Power. Power supply for the boost converter and portions of the Class D amplifier.	_	_
VSNS+	F1	VSPK	Ι	Voltage Sense Input. Sense voltage for signal originating from OUT+.	—	
VSNS-	E1	VSPK	Ι	Voltage Sense Input. Sense voltage for signal originating from OUT	_	—
VSPK	C1, D1		Ι	Amplifier Power. Power supply for the Class D amplifier's output stage.	—	

Table 1-1. WLCSP Pin Descriptions (Cont.)



2 Typical Connection Diagrams

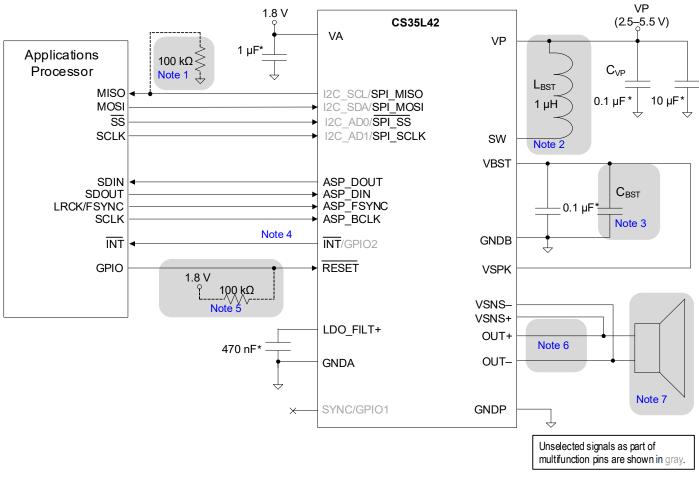


Figure 2-1. Typical Connection Diagram—Mono Configuration (Internal Boost Converter) and SPI Control



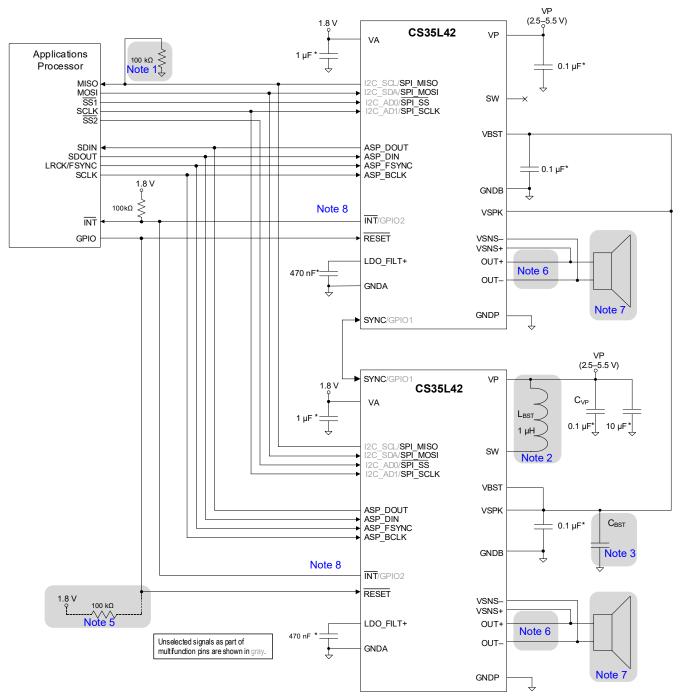


Figure 2-2. Typical Connection Diagram—Stereo Configuration with Shared Boost and SPI Control



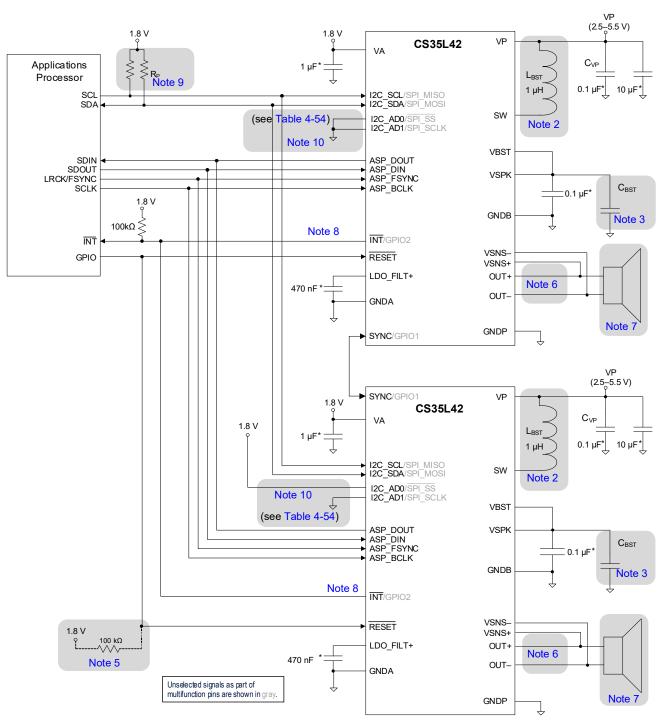
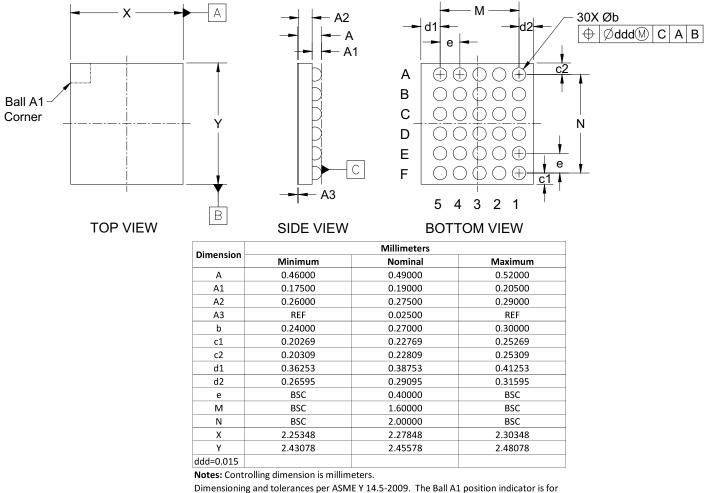


Figure 2-3. Typical Connection Diagram—Stereo Configuration with Separate Boost and I²C Control



3 Package Dimensions

3.1 WLCSP Package Dimensions



Dimensioning and tolerances per ASME Y 14.5-2009. The Ball A1 position indicator is for illustration purposes only. Dimension "b" applies to the solder sphere diameter and is measured at the maximum solder sphere diameter, parallel to primary Datum C. X/Y Tolerances can apply to an individual edge increasing or decreasing by 25um.

Figure 3-1. WLCSP Package Dimensions



4 Package Marking



Top Side Brand

Line 1: Customer-designated part number Line 2: Package mark Line 3: Country of origin Line 4: Encoded Wafer/Device ID

RR = Device revision code LL = Lot sequence code YY = Year of manufacture WW = Work week of manufacture

Figure 4-1. Package Marking



5 Ordering Information

Table 5-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	I/O Option	Order Number
CS35L42	11 V Boosted Mono Class D Amplifier with DSP	30-ball WLCSP	Yes	Commercial	-40°C to +85°C	Tape and Reel	1.8 V	CS35L42-CWZR

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to www.cirrus.com.

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